

Husain Parvez · Habib Mehrez

Application-Specific Mesh-based Heterogeneous FPGA Architectures

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Yao-Wen Chang

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Application-Specific Mesh-based Heterogeneous FPGA Architectures Husain Parvez,Habib Mehrez,2010-11-05 This book presents a new exploration environment for mesh based heterogeneous FPGA architectures It describes state of the art techniques for reducing area requirements in FPGA architectures which also increase performance and enable reduction in power required Coverage focuses on reduction of FPGA area by introducing heterogeneous hard blocks such as multipliers adders etc in FPGAs and by designing application specific FPGAs Automatic FPGA layout generation techniques are employed to decrease non recurring engineering NRE costs and time to market of application specific heterogeneous FPGA architectures

Tree-based Heterogeneous FPGA Architectures Umer Farooq,Zied Marrakchi,Habib Mehrez,2012-05-14 This book presents a new FPGA architecture known as tree based FPGA architecture due to its hierarchical nature This type of architecture has been relatively unexplored despite their better performance and predictable routing behavior as compared to mesh based FPGA architectures In this book we explore and optimize the tree based architecture and we evaluate it by comparing it to equivalent mesh based FPGA architectures

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Three-Dimensional Design Methodologies for Tree-based FPGA Architecture Vinod Pangracious,Zied Marrakchi,Habib Mehrez,2015-06-25 This book focuses on the development of 3D design and implementation methodologies for Tree based FPGA architecture It also stresses the needs for new and augmented 3D CAD tools to support designs such as the design for 3D to manufacture high performance 3D integrated circuits and reconfigurable FPGA based systems This book was written as a text that covers the foundations of 3D integrated system design and FPGA architecture design It was written for the use in an elective or core course at the graduate level in field of Electrical Engineering Computer Engineering and Doctoral Research programs No previous background on 3D integration is required nevertheless fundamental understanding of 2D CMOS VLSI design is required It is assumed that reader has taken the core curriculum in Electrical Engineering or Computer Engineering with courses like CMOS VLSI design Digital System Design and Microelectronics Circuits being the most important It is accessible for self study by both senior students and professionals alike

Reconfigurable Computing: Architectures, Tools and Applications Andreas Koch,Ram Krishnamurthy,John McAllister,Roger Woods,Tarek El-Ghazawi,2011-03-15 This book constitutes the refereed proceedings of the 7th International Symposium on Reconfigurable Computing Architectures Tools and Applications ARC 2011 held in Belfast UK in March 2011 The 40 revised papers presented consisting of 24 full papers 14 poster papers and the abstracts of

2 plenary talks were carefully reviewed and selected from 88 submissions The topics covered are reconfigurable accelerators design tools reconfigurable processors applications device architecture methodology and simulation and system architecture

Proceedings of the 5th International Workshop on Reconfigurable Communication-centric Systems on Chip 2010 - ReCoSoC'10 Michael Hübner,2010

Low-power Heterogeneous Reconfigurable Digital Signal Processors with Energy-efficient Interconnect Network Hui Zhang (Ph.D.),2004

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2001) ,2001 Comprises 20 papers selected for presentation at the Async 2001 conference in March 2001 as well as three invited presentations from industry researchers Papers were divided into seven sessions systems arithmetic experiments synthesis and verification handshaking communication architecture and performance analysis and optimization The invited talks are titled Asynchronous Design and the Pursuit of Low Power Where Are the Async Millionaires and Testing

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information on the design and testing of computer hardware presented at the 2002 IEEE Computer Society Annual

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Customizable Virtual FPGA Răzvan Peter Figuli,2017 Routing architectures and algorithms for field-programmable

gate arrays Yao-Wen Chang,1996 A Field Programmable Gate Array FPGA is a re programmable logic device that

implements multi level logic FPGA s can be configured by designers at their sites eliminating the time consuming fabrication step and thus result in low prototyping cost and short manufacturing time These advantages have made FPGA s very popular since their first introduction in mid 1980s However as a relatively new technology FPGA architectures are constantly evolving and current approaches for designing the traditional Application Specific Integrated Circuits ASIC s do not apply to

FPGA s well Thus it is desirable to consider architectures for FPGA design and develop FPGA specific computer aided design tools Logic circuits are implemented in an FPGA by partitioning logic into logic modules and then interconnecting the

modules FPGA interconnection resources consist of pre fabricated wire segments and programmable switches Routing in

FPGA is performed by programming the switches to connect the wire segments The programmable switches usually have high resistance and capacitance and consume a large amount of area Due to the area and delay constraint the number of

switches that can be placed in a switch module is usually limited implying limited routability It is thus of importance to design switch modules that maximize routability under the area and delay constraints This thesis focuses on two closely

related issues for FPGA's routing and its architectures Routing architecture There are two types of switch modules switch blocks and switch matrices We present techniques for designing and analyzing a class of universal switch blocks which accommodate all types of nets routed through them and show theoretically and experimentally that they outperform the switch blocks currently available For switch matrices we show the nonexistence of their universality analyze the routability of commercially available architectures and present effective approaches for designing good switch matrices Routing We show a class of network flow based approximation algorithms for a switch module routing problem and prove that they have guaranteed constant performance bounds Solutions to this switch module routing problem pave the way for developing a novel congestion metric for FPGA global routing Experimental results show that the new metric significantly improves a router's area performance Area and speed are two most important concerns in router design To consider area and speed simultaneously we study a model of timing driven routing arising from the special properties of FPGA routing architectures We explore the complexity of this problem and present efficient and effective approximation algorithms for the problem

Architecture and CAD for Nanoscale and 3d FPGA Chen Dong, 2011 FPGAs field programmable gate arrays are attractive alternatives compared to ASICs application specific integrated circuits for significantly lowering amortized manufacturing costs and dramatically improving design productivity The architecture of an FPGA is very regular It is relatively easy to design a highly optimized tile with consideration of various manufacturing related issues and then to replicate it many times across the chip The configurability of FPGAs also enables yield improvement and defect tolerance However FPGAs are still facing serious challenges in terms of delay power consumption and logic density compared to ASICs FPGA is estimated to be over twenty times less efficient in logic density over three times worse in delay and over ten times higher in power consumption compared to a functionally equivalent ASIC One promising way to improve FPGA performance is to incorporate three dimensional 3D integration which increases the number of active layers and optimizes the interconnect network vertically Another solution is to apply novel nanoelectronic materials nanomaterials and devices This dissertation introduces three novel reconfigurable architectures named 3D nFPGA FPCNA field programmable carbon nanotube array and NEM FPGA nanoelectromechanical FPGA which utilize 3D integration techniques and new nanoscale materials synergistically Customized CAD flows that consider process variation have been developed for different architectures to evaluate their potential performances Also described is a 3D variation aware routing flow which is an essential tool for future 3D FPGA architecture exploration 3D nFPGA is based on CMOS complementary metal oxide semiconductor and nano hybrid techniques that incorporate nanomaterials such as nanowire crossbars and carbon nanotube bundles into the CMOS fabrication process Using unique features of FPGAs and a novel 3D stacking method enabled by the application of nanomaterials 3D nFPGA obtains a 4-7 footprint reduction comparing to the traditional CMOS based 2D FPGAs The performance and power of 3D nFPGA driven by the 20 largest MCNC microelectronics center of North Carolina

benchmarks have been evaluated. Results demonstrate that 3D nFPGA is able to provide a performance gain of 2.67 with a small power overhead compared to the traditional 2D FPGA. FPCNA includes lookup tables created entirely from continuous carbon nanotube CNT ribbons. To determine the performance of the building blocks variation aware physical design tools are used with statistical static timing analysis SSTA that can handle both Gaussian and non Gaussian random variables. A 2.757 performance improvement is seen over an equivalent CMOS FPGA at a 95% yield. In addition FPCNA offers a 5.7 footprint reduction compared to a baseline FPGA. 3D NEM FPGA is the architecture that utilizes nanoelectromechanical NEM relays and 3D integration techniques synergistically. This proposed architecture has unique features including a hybrid CMOS/NEM FPGA lookup table LUT and configurable logic block CLB. NEM based switch block SB and connection block CB and face to face 3D stacking. This architecture also has a built in feature called direct link which takes advantage of the short vertical wire length provided by 3D stacking to further enhance performance. An overall 46.3% critical path delay reduction has been observed compared to its CMOS counterpart. To maximize the potential performance gain of 3D integrated circuit architectures an SSTA engine was developed to deal with both uncorrelated and correlated variations in 3D FPGAs. The effects of intra die and inter die variation are considered. Using the 3D physical design tool TPR as a base a new 3D routing algorithm is developed which improves the average performance of two layer designs by over 22% and three layer designs by over 27%.

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