

### 3.3 Instruction set summary

This section provides information on:

- *Cortex-M4 instructions*
- *Load/store timings on page 3-11*
- *Binary compatibility with other Cortex processors on page 3-12*

#### 3.3.1 Cortex-M4 instructions

The processor implements the ARMv7-M Thumb instruction set. Table 3-1 shows the Cortex-M4 instructions and their cycle counts. The cycle counts are based on a system with zero wait states.

Within the assembler syntax, depending on the operation, the <op2> field can be replaced with one of the following options:

- a simple register specifier, for example `Rn`
- an immediate shifted register, for example `Rn, LSL #4`
- a register shifted register, for example `Rn, LSL Rn`
- an immediate value, for example `#0xE000E000`

For brevity, not all load and store addressing modes are shown. See the *ARMv7-M Architecture Reference Manual* for more information.

Table 3-1 uses the following abbreviations in the Cycles column:

- P** The number of cycles required for a pipeline refill. This ranges from 1 to 3 depending on the alignment and width of the target instruction, and whether the processor manages to speculate the address early.
- B** The number of cycles required to perform the barrier operation. For DSB and DMB, the minimum number of cycles is zero. For ISB, the minimum number of cycles is equivalent to the number required for a pipeline refill.
- N** The number of registers in the register list to be loaded or stored, including PC or LR.
- W** The number of cycles spent waiting for an appropriate event.

Table 3-1 Cortex-M4 instruction set summary

Operation	Description	Assembler	Cycles
Move	Register	MOV Rd, <op2>	1
	16-bit immediate	MOVW Rd, #<imm>	1
	Immediate into top	MOVT Rd, #<imm>	1
	To PC	MOV PC, Rn	1 + P
Add	Add	ADD Rd, Rn, <op2>	1
	Add to PC	ADD PC, PC, Rn	1 + P
	Add with carry	ADC Rd, Rn, <op2>	1
	Form address	ADR Rd, <label>	1

# Arm Cortex M4 Instruction Set

**F Rizvi**

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### **Table of Contents Arm Cortex M4 Instruction Set**

1. Understanding the eBook Arm Cortex M4 Instruction Set
  - The Rise of Digital Reading Arm Cortex M4 Instruction Set
  - Advantages of eBooks Over Traditional Books
2. Identifying Arm Cortex M4 Instruction Set
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Arm Cortex M4 Instruction Set
  - User-Friendly Interface
4. Exploring eBook Recommendations from Arm Cortex M4 Instruction Set
  - Personalized Recommendations
  - Arm Cortex M4 Instruction Set User Reviews and Ratings

- Arm Cortex M4 Instruction Set and Bestseller Lists
- 5. Accessing Arm Cortex M4 Instruction Set Free and Paid eBooks
  - Arm Cortex M4 Instruction Set Public Domain eBooks
  - Arm Cortex M4 Instruction Set eBook Subscription Services
  - Arm Cortex M4 Instruction Set Budget-Friendly Options
- 6. Navigating Arm Cortex M4 Instruction Set eBook Formats
  - ePUB, PDF, MOBI, and More
  - Arm Cortex M4 Instruction Set Compatibility with Devices
  - Arm Cortex M4 Instruction Set Enhanced eBook Features
- 7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Arm Cortex M4 Instruction Set
  - Highlighting and Note-Taking Arm Cortex M4 Instruction Set
  - Interactive Elements Arm Cortex M4 Instruction Set
- 8. Staying Engaged with Arm Cortex M4 Instruction Set
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Arm Cortex M4 Instruction Set
- 9. Balancing eBooks and Physical Books Arm Cortex M4 Instruction Set
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Arm Cortex M4 Instruction Set
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine Arm Cortex M4 Instruction Set
  - Setting Reading Goals Arm Cortex M4 Instruction Set
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Arm Cortex M4 Instruction Set
  - Fact-Checking eBook Content of Arm Cortex M4 Instruction Set
  - Distinguishing Credible Sources

13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
14. Embracing eBook Trends
  - Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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