



Part numbers

# 555

Spare parts

Ersatzteile

Pièces détachées

Reserve onderdelen

Repuestos

Reservdelar

# 555 Parts Manual

**Joseph D. Moell, Thomas N. Curlee**

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web the i 2c module contains an independent i 2c master logic and a i 2c slave logic which generates interrupts based on their events in the multi master systems the user software is simply partitioned into the master controller and the slave controller when the i 2c master logic is active the slave logic also remains active detecting the

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web i2c master h this header contains i o definitions selection and timing clock speed settings used for the master i2c interface this file also includes prototypes of master i2c functions i2c master c this source file contains master i2c function implementations file

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web the i 2 c master is byte oriented and interrupt based the number of interrupts generated is kept at a minimum by automatic handling of most incidents the software driver complexity and code size are reduced by auto triggering of operations and a special smart mode which can be enabled by the smart mode enable bit in the control b register

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web this example shows how the microcontroller configured in i 2 c host mode writes to and reads data from an mcp23008 8 bit i 2 c i o expander client device addressed in 7 bit mode using interrupts

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web control of the i 2 c bus may be taken when the p bit is set or the bus is idle in firmware controlled master mode user code conducts all i 2 c bus operations based on start and stop bit condition detection start and stop condition detection is

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web lbidirectional i2c stands for inter integrated circuit communications i2c is implemented in the picmicro by a hardware module called the master synchronous serial port known as the mssp module

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web c bus is a two wire serial bus with multiple possible masters and multiple possi ble slaves connected to each other through two wires the two wires consists of a clock line scl and a data line sda with both lines being bi directional

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web nov 7 2016 ds90003159b page 2 2017 microchip technology inc i<sup>2</sup>c protocol overview the i<sup>2</sup>c module follows the phillips i<sup>2</sup>c specification the module provides a bidirectional master slave synchronous interface between the pic microcontroller and other i<sup>2</sup>c supported devices these devices are connected via a two wire serial bus

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web the master synchronous serial port mssp is an integrated serial communications module the mssp contains two sub modules spi serial peripheral interface i<sup>2</sup>c inter integrated circuit the inter integrated circuit commonly referred to as i<sup>2</sup>c is a synchronous two wire bidirectional serial communications bus

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web jun 23 2016 key features of the i<sup>2</sup>c module include the following independent master and slave logic multi master support which prevents message losses in arbitration detects 7 bit and 10 bit device addresses with configurable address masking in slave mode detects general call addresses as defined in the i<sup>2</sup>c protocol automatic sclx clock

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