

ITERATIVE ARRAYS OF LOGICAL CIRCUITS

FREDERICK C. HENNIE, JR.

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Clifford Allen Isberg

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Frederick C. Hennie Iii,2013-03 **Iterative Arrays of Logical Circuits** Frederick C. Hennie,2003-02 An exploration of the techniques for analyzing the behavior of one and two dimensional iterative networks formed of discrete or logical elements showing that most questions about the behavior of iterative systems are recursively undecidable **Iterative Arrays Of Logical Circuits** F.C. Hennie, *A Functional Characterization of Iterative Arrays of Logical Circuits* Clifford Allen Isberg,1964 *ITERATIVE ARRAYS OF LOGICAL CIR- CIRCUITS* ,1961 **Scientific and Technical Aerospace Reports** ,1967 Lists citations with abstracts for aerospace related reports obtained from world wide sources and announces documents that have recently been entered into the NASA Scientific and Technical Information Database **The Essence of Logic Circuits** Stephen H. Unger,1997 Today designing a state of the art circuit means knowing how to pack more and more logic on a chip Featuring an extensive introductory material this complete carefully organized guide brings you valuable information on designing modern logic circuits from gates switches and other basic elements to meet the rising demands on modern circuit technology THE ESSENCE OF LOGIC CIRCUITS allows computer scientists and students to start from scratch and gain a comprehensive understanding of most important topics in the field [Testing of Digital Systems](#) N. K. Jha,S. Gupta,2003-05-08 Device testing represents the single largest manufacturing expense in the semiconductor industry costing over 40 billion a year The most comprehensive and wide ranging book of its kind Testing of Digital Systems covers everything you need to know about this vitally important subject Starting right from the basics the authors take the reader through automatic test pattern generation design for testability and built in self test of digital circuits before moving on to more advanced topics such as IDDQ testing functional testing delay fault testing memory testing and fault diagnosis The book includes detailed treatment of the latest techniques including test generation for various fault models discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system on a chip test synthesis Written for students and engineers it is both an excellent senior graduate level textbook and a valuable reference *NASA SP.* ,1965

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