



14 Regional Convention Notebook

Yan Bai

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web for sample syntax and a list of vhdl statements supported by the vhdl synthesizer see appendix a quick reference for a

list of exceptions and constraints on the vhdl synthesizer s support of vhdl see appendix b limitations this chapter shows you the structure of a vhdl design and then

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web basic logic gates esd chapter 2 figure 2 3 every vhdl design description consists of at least one entity architecture pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

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