



# User Manual Suzuki Burgman 400

**Léo Pomar**



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### **User Manual Suzuki Burgman 400 Introduction**

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systems had direct controls that were not as efficient and required higher voltage but newer systems use control boards to communicate with different components calculate for best performance and then directly control

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web section a variable speed furnace control boards hk42fz003 hk42fz012 hk42fz055 hk42fz056 hk42fz064 hk42fz057 hk42fz058 hk42fz088 hk42fz089 step action yes no go to 1 turn power off remove blower access panel and disconnect r thermostat lead 2 2 turn the power on and depress the door switch

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web feb 6 2021 in this hvac training video i show how the blower motor is controlled by the relays on a furnace control board i show wiring diagrams and test the board with a multimeter supervision is needed

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web aug 22 2017 the more common control board at least in newer units is the integrated furnace control board this controls the same things as the simple ignition control board but it controls the furnace blower as well ultimately it is the simple ignition control board and the fan control board in one step by step sequence

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web control circuits for hvac systems the relay in the above control diagram controls a blower motor as shown furthermore this particular relay is controlled by the thermostat the 24 volt neutral leg will run from the transformer then go to one side of a coil on the relay the 24 hot leg of the transformer will go through the thermostat

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web the next step is to follow the lines and see where they go in this example diagram you can see that one leg of the secondary connects to the r terminal on the control board and the other leg connects to the c terminal in this example there s actually a c terminal present but that will not always be the case especially in old models

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web the i2c module contains an independent i2c master logic and a i2c slave logic which generates interrupts based on their events in the multi master systems the user software is simply partitioned into the master controller and the slave controller when the i2c master logic is active the slave logic also remains active detecting the

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web i2c master h this header contains i o definitions selection and timing clock speed settings used for the master i2c interface this file also includes prototypes of master i2c functions i2c master c this source file contains master i2c function implementations file

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web i2c module modes and features the i2c module provides the following operational modes and features master mode slave mode with byte nacking multi master mode dedicated receive and transmit buffers up to four dedicated slave address registers 1

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web the i2c master is byte oriented and interrupt based the number of interrupts generated is kept at a minimum by automatic handling of most incidents the software driver complexity and code size are reduced by auto triggering of operations and a special smart mode which can be enabled by the smart mode enable bit in the control b register

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web mar 4 2022 sam sercom i2c master driver copyright c 2012 2018 microchip technology inc and its subsidiaries include i2c common h include sercom h include pinmux h include sercom interrupt h define pinmux default 0

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web this example shows how the microcontroller configured in i2c host mode writes to and reads data from an mcp23008 8 bit i2c i o expander client device addressed in 7 bit mode using interrupts

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web control of the i2c bus may be taken when the p bit is set or the bus is idle in firmware controlled master mode user code conducts all i2c bus operations based on start and stop bit condition detection start and stop condition detection is

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web lbidirectional i2c stands for inter integrated circuit communications i2c is implemented in the picmicro by a hardware

module called the master synchronous serial port known as the mssp module  
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web i<sup>2</sup>c bus is a two wire serial bus with multiple possible masters and multiple possible slaves connected to each other through two wires the two wires consists of a clock line scl and a data line sda with both lines being bi directional

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web nov 7 2016 ds90003159b page 2 2017 microchip technology inc i2c protocol overview the i2c module follows the phillips i2c specification the module provides a bidirectional master slave synchronous interface between the pic microcontroller and other i2c supported devices these devices are connected via a two wire serial bus

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web the master synchronous serial port mssp is an integrated serial communications module the mssp contains two sub modules spi serial peripheral interface i2c inter integrated circuit the inter integrated circuit commonly referred to as i2c is a synchronous two wire bidirectional serial communications bus

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web jun 23 2016 key features of the i2c module include the following independent master and slave logic multi master support which prevents message losses in arbitration detects 7 bit and 10 bit device addresses with configurable address masking in slave mode detects general call addresses as defined in the i2c protocol automatic sclx clock

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web the i2c bus is a multi master serial data communication bus microcontrollers communicate in a master slave environment where the master devices initiate the communication and the devices are selected through addressing i2c operates with one or more master devices and one or more slave devices

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subsidiaries include asf h define data length 10 packet data referenced by main and setup dma descriptor define slave address 0x12 referenced by main define timeout 1000

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